Comparative Study and Analysis for the Design of Random Access Memory using different CMOS Technologies

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Abstract— RAM has become a major component in many VLSI Chips due to their large storage density and small access time. RAM has become the topic of research due to the rapid development for low power, low voltage small area and high speed during recent years due to increase demand for notebooks, laptops, high speed memory, Memory cards and hand held communication devices. RAMs are widely used for mobile applications as both on chip and off chip memories, because of their ease of use and low standby leakage. In most of the digital circuits, CMOS based design is allowed to be used in practice. Generally, CMOS stands for Complementary Metal Oxide Semiconductor Field Effect Transistor that is, considered to be as combination of both PMOS as well as NMOS. In CMOS based design, symmetry should be followed in circuit operation. Most of the complex circuits are allowed to design in CMOS, however, there are several drawbacks present in this complementary based design. Also, RAM cell read stability and write-ability is major concern in nanometer CMOS technologies, due to the supply voltage scaling. CMOS has superior properties in terms of power consumption, leakage power, delay etc. The objective of this work mainly focus on study and analysis of random access memory using CMOS technology, CMOS find the parameters such as average power, delay, Gate length, Power dissipation and leakage current.

Keywords — CMOS, RAM cell, Power dissipation, Read Delay, Write Delay, Leakage current, PMOS, NMOS.

I. INTRODUCTION.

Random-access memory (RAM) is a type of storage for computer systems that makes it possible to access data very quickly in random order. RAM is the place in a computer where the operating system, application programs, and data in current use are kept so that they can be quickly reached by the computer's processor. RAM is much faster to read from and write to than the other kinds of storage in a computer, the hard disk, floppy disk, and CD-ROM. However, the data in RAM stays there only as long as your computer is running. When you turn the computer off, RAM loses its data. When you turn your computer on again, your operating system and other files are once again loaded into RAM, usually from your disk. RAM is small, both in physical size (it's stored in microchips) and in the amount of data it can hold. It's much smaller than your hard disk. A typical computer may come with 256 million bytes of RAM and a hard disk that can hold 40 billion bytes.

Figure 1. Basic Random Access Memory Structure.
while the storage capacity of the hard disk drive can be several hundred GB or even one TB (terabyte).

II. TYPE OF RANDOM ACESS MEMORY

A. Static RAM (SRAM).
Static RAM (SRAM) uses four or more transistors to store a single bit of data. Different combinations represent a state of zero or one. The term static refers to the fact that it maintains its current state without having to be refreshed on a regular basis.

B. Dynamic RAM (DRAM).
Dynamic RAM (DRAM) is by far the most widely used. It stores each bit of data using a transistor and capacitor pair. Combined, they represent a single memory cell. The capacitor holds a low or a high charge, representing a zero or one, respectively.

C. Resistive random access memory (RRAM).
Resistive random access memory (RRAM) is being developed by several companies, but fabrication usually requires high-temperatures or voltages, making production difficult and expensive. The Rice researchers have shown a way to make RRAM at room temperature and with far lower voltages. RRAM stores bits using resistance. Each bit requires less space, increasing the amount of information that can be stored in a given area.

D. Ferroelectric RAM (FRAM).
FRAM is a random-access memory similar in construction to DRAM but uses a ferroelectric layer instead of a dielectric layer to achieve non-volatility. FeRAM is one of a growing number of alternative non-volatile random-access memory technologies that offer the same functionality as flash memory. FeRAM advantages over flash include: lower power usage, faster write performance and a much greater maximum number of write-erase cycles (exceeding $10^{16}$ for 3.3 V devices). Disadvantages of FeRAM are much lower storage densities than flash devices, storage capacity limitations, and higher cost.

E. Nanotube RAM (NRAM).
NRAM has an almost infinite number of write cycles, and is thousands of times faster than flash A new type of non-volatile memory known as Nano- RAM (NRAM) it’s based on carbon nanotube and sports DRAM speed is now being produced in seven fabrication plants in various parts of the world. According to Nantero, the company that invented NRAM, it also has more than a dozen corporate customers lined up to begin experimenting with the memory once it begins rolling off production lines.

III. DESING OF RANDOM ACESS MEMROY.
Static random-access memory (SRAM or static RAM) is uses bistable latching circuitry to store each bit. The term static differentiates it from dynamic RAM (DRAM) which must be periodically refreshed. SRAM exhibits data remanence but it is still volatile in the conventional sense that data is eventually lost when the memory is not powered. In a 6 transistor Static RAM cell, the two cross-coupled PMOS pull-up devices retain the value written into a cell. These cross-coupled p-devices are designed to be strong enough to retain a value in the cell indefinitely without any external refresh mechanism. However, if the p-devices are too weak due to a fabrication defect or a connection to either of the p-devices is missing, the static RAM (cell will no longer be able to hold its data indefinitely.

Low power SRAM cell may be designed by using cross-coupled CMOS inverters shown in figure 1. The most important advantage of this circuit topology is that the static power dissipation is very small essentially; it is limited by small leakage current. Other advantages of this design are high noise immunity due to larger noise margins, and the ability to operate at lower power supply voltage. The major disadvantage of this topology is larger cell size.

Figure 2. Cross couple Invertor SRAM Cell

The circuit structure of the full CMOS static RAM cell is shown in Figure 3. The memory cell consists of simple CMOS inverters connected back to back, and two access transistors. The access transistors are turned on whenever a word line is activated for read or write operation, connecting the cell to the complementary bit line columns.

Figure 3. Schematic of 6T FULL CMOS SRAM Cell.
During hold, VWL is held low and the BLs are left floating or driven to VDD. Each bit in an SRAM is stored on four transistors that form two cross-coupled inverters. This storage cell has two stable states, which are used to denote 0 and 1. Two additional access transistors serve to control the access to a storage cell during read and write operations. A typical SRAM uses six MOSFETs to store each memory bit and the explanation here is based on the same. Access to the cell is enabled by the word line which controls the two access transistor M5 and M6 which, in turn, control whether the cell should be connected to the bit lines: BL and BLB. They are used to transfer data for both read and write operations. Although it is not strictly necessary to have two bit lines, both the signal and its inverse are typically provided to improve noise margins. During read accesses, the bit lines are actively driven high and low by the inverters in the SRAM cell. This improves SRAM bandwidth compared to DRAMs. A SRAM cell has three different states it can be in: standby where the circuit is idle, reading when the data has been requested and writing when updating the contents.

IV. READ & WRITE OPERATION OF SRAM MEMORY.
A. Standby Mode SRAM cell.
Standby Mode (the circuit is idle) in standby mode word line is not asserted (word line=0), so pass transistors N3 and N4 which connect 6t cell from bit lines are turned off. It means that cell cannot be accessed. The two cross coupled inverters formed by N1-N2 will continue to feedback each other as long as they are connected to the supply, and data will hold in the latch.

B. Read Mode of SRAM cell.
Besides the read stability for the SRAM cell, a reasonable write-trip point is equally important to guarantee the write ability of the cell without spending too much energy in pulling down the bitline voltage to 0 V. The write-trip point defines the maximum voltage on the bit-line, needed to flip the cell content. The write-trip point is mainly determined by the pull-up ratio of the cell while the read stability is determined by the cell ratio of cell; this results in the well-known conflicting design criteria. The SRAM N-curve can also be used as alternative for the write-ability of the cell, since it gives indications on how difficult or easy it is to write the cell.

C. Write Mode of SRAM cell.
Write Mode (updating the contents) Assume that the cell is originally storing a 1 and we wish to write a 0. To do this, the bit line is lowered to 0V and bit bar is raised to VDD, and cell is selected by raising the word line to VDD.

V. COMPARATIVELY ANALYSIS FOR DIFFERENT CMOS TECHNOLOGY.
A. Recent trends in CMOS Technology.
Firstly, we give an overview of the evolution of important parameters such as the integrated circuit (IC) complexity, the gate length, switching delay and supply voltage with a prospective vision down to the 22 nm CMOS technology. The trend of CMOS technology improvement continues to be driven by the need to integrated more functions in a given silicon area. Table 1 gives an overview of key parameters for technological nodes from 180 nm introduced in 1999, down to 22 nm, which is supposed to be in production around 2011.
The mobility improvement exhibits a linear dependence with the tensile film thickness. A 80 nm film has resulted in a 10% saturation current improvement in Intel’s 90nm technology [Ghani]. The strain may also be applied from the bottom with a uniform layer of an alloy of silicon and germanium (SiGe).

In a similar way, compressing the lattice slightly speeds up the p-type transistor, for which current carriers consist of holes. The combination of reduced channel length, decreased oxide thickness and strained silicon achieves a substantial gain in drive current for both nMOS and pMOS devices.

C. 65 nm Technology.

For this 65nm technology we use 1.2nm SiON gate oxide, which is not scaled from Intel’s previous 90nm technology in order to avoid an increase in gate oxide leakage. Maintaining constant gate oxide thickness while scaling gate length to 35nm provides ~20% reduction in gate capacitance, a significant factor in improving performance and reducing active power. Transistor drive currents are increased by means of ultra-shallow junctions and enhanced channel strain. Interconnect density and performance are improved with an added interconnect layer and by use of a low-k carbon-doped oxide layer and a lower-k etch stop layer for low capacitance, and Cu interconnect for low resistance. 193nm lithography combined with APSM mask technology enables aggressive design rule scaling. The SRAM cell size is scaled to 0.57 µm2 with stable low voltage operating characteristics.

The 65nm low power technology offering a dual gate oxide process, multiple Vt devices at a nominal operating voltage of 1.2V, a nine level hierarchical Cu interconnect back-end of line process with low k dielectrics and 0.676 mm2 and 0.54mm2 SRAM cells, optimized for performance and density, respectively. The key focus of this technology has been low cost, process simplicity and power reduction. A gate dielectric with an nft leakage current as low as 15pA/mum and with exceptional reliability characteristics has been demonstrated.

D. 45 nm Technology.

The 45nm introducing new high-k materials into the gate stack, for the purpose of reducing leakage current density. As of 2007, however, both IBM and Intel have announced that they have high-k dielectric and metal gate solutions, which Intel considers to be a fundamental change in transistor design. Demonstration chips using 45nm technology have been reported starting in 2004. Mass market manufacturing with this technology is scheduled for late 200. The devices used in this study are 45 nm low-power CMOS and 65 nm CMOS devices from IBM. The 45 nm devices all have a gate length of 30 nm and VDD= 1.1 V, while the 65 nm devices have a gate length of 35 nm and VDD= 1 V.

Table 1: Comparative analysis of CMOS Parameter.

<table>
<thead>
<tr>
<th>Technology</th>
<th>90 nm</th>
<th>65 nm</th>
<th>45 nm</th>
<th>32 nm</th>
<th>22 nm</th>
<th>14 nm</th>
<th>10 nm</th>
</tr>
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<tr>
<td>Years</td>
<td>2003</td>
<td>2005</td>
<td>2007</td>
<td>2009</td>
<td>2011</td>
<td>2013</td>
<td>2015</td>
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<tr>
<td>Device's</td>
<td>IBM</td>
<td>IBM</td>
<td>Xeon</td>
<td>Intel Core7</td>
<td>Phone</td>
<td>TSMC</td>
<td></td>
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<tr>
<td>Frequency</td>
<td>1.8 GHz</td>
<td>1.8 GHz</td>
<td>1.8n GHz</td>
<td>1.8 GHz</td>
<td>1.8-3.0 GHz</td>
<td>3.8 GHz</td>
<td>3.8 GHz</td>
</tr>
<tr>
<td>Gate Length</td>
<td>50 nm</td>
<td>55 nm</td>
<td>30 nm</td>
<td>25 nm</td>
<td>18 nm</td>
<td>12 nm</td>
<td>9 nm</td>
</tr>
<tr>
<td>Gate Material</td>
<td>Poly</td>
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<td>Metal</td>
<td>Metal</td>
<td>Metal</td>
<td>Metal</td>
<td>Dual</td>
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<tr>
<td>Kgate /nm²</td>
<td>0.4</td>
<td>0.8</td>
<td>1.5</td>
<td>2.8</td>
<td>5.2</td>
<td>9.0</td>
<td>16.0</td>
</tr>
<tr>
<td>Memory density</td>
<td>1.3</td>
<td>0.6</td>
<td>0.3</td>
<td>0.15</td>
<td>0.08</td>
<td>0.06</td>
<td>0.06</td>
</tr>
</tbody>
</table>

E. 32 nm Technology.

The Prototypes using 32 nm technologies first emerged in the mid-2000s. In 2004, IBM demonstrated a 0.143 µm² SRAM cell with a poly gate pitch of 135 nm, produced using electron-beam lithography and photolithography on the same layer. It was observed that the cell's sensitivity to input voltage fluctuations degraded significantly at such a small scale. The Full 32 nm CMOS technology for high data rate and low operating power applications using a conventional high-k with single metal gate stack. High speed digital transistors are demonstrated 22% delay reduction for ring oscillator (RO) at same power versus previous SiON technology.

F. 22 nm Technology.

The 22 nanometer (22 nm) node is the process step following the 32 nm in CMOS semiconductor device fabrication. The typical half-pitch for a memory cell using the process is around 22 nm. It was first introduced by semiconductor companies in 2008 for use in memory products, while first consumer-level CPU deliveries started in April 2012. The down-scaling is still the most important and effective way for achieving the high-performance logic CMOS operation with low power, regardless of its concern for the technological difficulties, and thus, the past shrinking trend of the gate-length has been very aggressive.
G. 14 nm Technology.
The 14nm semiconductor device fabrication node is the technology node following the 22 nm/ (20 nm) node. 14 nm resolutions are difficult to achieve in a polymeric resist, even with electron beam lithography. In addition, the chemical effects of ionizing radiation also limit reliable resolution to about 30 nm, which is also achievable using current state-of-the-art immersion lithography. Hard mask materials and multiple patterning are required. For technology node 32nm effective gate length is 25nm with High K gate dielectric. There may exist several variants of the 32-nm process technology. One corresponds to the highest possible speed, at the price of a very high leakage current. This technology is called “High speed” as it is dedicated to applications for which the highest speed is the primary objective: fast microprocessors, fast DSP, etc.

H. 10 nm Technology.
In semiconductor fabrication, the International Technology Roadmap for Semiconductors (ITRS) defines the 10 nanometer (10 nm) node as the technology node following the 14 nm node. "10 nm class" denotes chips made using process technologies between 10 and 20 nanometers. As of 2016, 10 nm devices are still under commercial development. The different software used to allows us to design and simulate an integrated circuit at physical description level. The package contains a library of common logic and analog ICs to view and simulate. It also includes all the commands for a mask editor as well as original tools never gathered before in a single module such as 2D and 3D process view, Verilog compiler, tutorial on MOS devices. You can gain access to Circuit Simulation by pressing one single key. The electric extraction of your circuit is automatically performed and the analog simulator produces voltage and current curves immediately.

VI. CONCLUSION.
This paper introduced the comparative study and analysis for the design of random access memory by using different CMOS technologies also comparison of parameters like performance, power consumption, delay are as desired. Also comparison analysis of frequency, area, gate length, gate material, Kgate/mm2, memory point and gate atom is important for CMOS Technology. The RAM cell provide higher read and write noise margin. This paper tries to find out an efficient RAM memory cell with higher read and write stability at different technologies.
The different software is useful for study and analysis an integrated circuit at parametric level. In the estimated design, more emphases are given on power consumption, layout design and many more.

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References