Single Electron Encoded Logic Gates

N. Basanta Singh
Department of Electronics & Communication Engineering
Manipur Institute of Technology, Imphal, Manipur, India

ABSTRACT

Single electron technology has ultra-low power consumption and high integration density, which make them promising candidates as basic circuit elements of the future generation Integrated circuits. In this work, basic single electron encoded gates such as NOT, AND, OR, NAND and NOR are investigated using the threshold logic gate implementation approach, in which the Boolean logic values are encoded as absence or presence of one electron charge. These gates were used to implement a digital system. All proposed circuits are verified by means of SIMON 2 simulation software. Free energy history and stability analysis have verified the correct functioning of the circuit.

Index Terms — Coulomb blockade, Single electron technology, Threshold logic gate, Tunnel junction.

INTRODUCTION

The present CMOS technology may presumably be continued for some more years by the well-known scaling of structure geometry. However, there have been reports suggesting that the MOS transistor cannot shrink beyond certain limits dictated by its operating principle [1]. Over recent years this realization has led to exploration of possible successor technologies with greater scaling potential such as single electron technology. Single electronics is nothing but the controlled manipulation of the movement and position of a single or small number of electrons. Single Electron Technology is the most promising future technology to meet the demand for increase in density, performance and decrease in power dissipation in future VLSI circuits [2,3]. The ultimate limit in the operation of an electronic device is the manipulation of a single charge. Such a limit can be achieved in single electron technology. Single-electron devices retain their scalability even on an atomic scale. Therefore, if the single-electron devices are used as VLSI elements, it will have the attributes of extremely high integration and extremely low power consumption.

One of the challenges of single electron VLSI technology is the development of integrated circuits on the basis of single electron tunnelling. For this we need to develop logic gates and circuits that can be used for design and implementation of large circuits and systems. Research in Single electron technology has mainly occurred at the device, therefore limited innovation has occurred at the circuit and system level. There have been attempts to mould the technology to a CMOS-like design style by making devices that mimic the behaviour of the MOS transistor [4-8]. Such attempts make limited use of the potential of the single electron technology. Traditional digital logic circuits have been implemented by representing Boolean functions as a network of AND, OR and NOT logic gates. The performance of Boolean implementation might be severely affected by a large circuit depth and alternative solutions are required. A potential alternative to Boolean Logic is the Threshold Logic which makes use of a generalized basic building block named Threshold Logic Gate. A Boolean function, if realized as a network of threshold gates, can result in significantly fewer nodes and smaller network depth.

In this work, we first briefly discuss the basic physics of single electron technology. Design and simulation of single electron encoded basic logic gates such as NOT, OR, AND, NOR and NAND are described using Threshold Logic Gates. The gates are used to design and implement a digital systems. The gates and the system are verified by simulation using SIMON2 software.
THE BASIC PHYSICS OF SINGLE ELECTRON TECHNOLOGY

The basic component of single electron tunnelling transistor is the tunnel junction. A tunnel junction can be considered as two conductors separated by a thin layer of insulating material. A tunnel junction can be thought of as a leaky capacitor \[ C_j \] which is characterised by a capacitance \( C_j \) and a resistance \( R_j \), each of which depends on the physical size of the tunnel junction and the thickness of the insulator. The transport of electrons through a tunnel junction is called tunnelling. Electrons are considered to tunnel through a tunnel junction one after another \[9, 10\]. Even only one electron tunneling may produce a charge \( e/C \) across the tunnel junction (where \( C \) is total capacitance and \( e = 1.602 \times 10^{-19} \text{C} \)). The critical voltage \( V_c \), which is the threshold voltage needed across the tunnel junction, can be calculated with the equation

\[
V_c = \frac{e}{2(C + C_j)} \tag{1}
\]

Where \( C_j \) is the junction capacitance and \( C_e \) is the equivalent capacitance for remainder circuit as viewed from the tunnel junction’s perspective. Tunnel event will occur across the tunnel junction if and only if the voltage \( V_j \) across the tunnel junction is greater than or equal to \( V_c \), i.e. \( |V_j| \geq V_c \), otherwise the tunnel event cannot occur. The circuit will be in stable state if \( |V_j| < V_c \).

Threshold logic gates (TLG) are devices which can compute any linearly separable Boolean functions given by \[9\].

\[
Y = \text{sgn}\{F(X)\} = \begin{cases} 0 & \text{if } F(X) < 0 \\ 1 & \text{if } F(X) \geq 0 \end{cases} \tag{2}
\]

Where \( F(X) = \sum_{i=1}^{n} w_i x_i - T \) \tag{3}

In (2) and (3) \( \psi \) is the threshold value, \( x_i \) is the \( i^{th} \) input and \( \omega_i \) is the corresponding integer weight. If the weighted sum of inputs \( \sum_{i=1}^{n} w_i x_i \) is greater than or equal to \( \psi \), the gate produces logic 1 at the output; otherwise output will be logic 0. The Symbol and generic circuit implementation of \( n \) input TLG is shown in Figs. 1(a) and 1(b).

The input voltages \( V^p \) weighted by their input capacitances \( C^p \) are added to \( V_j \) and the input voltages \( V^n \) weighted by their input capacitances \( C^n \) are subtracted from \( V_j \). The critical voltage \( V_c \) of the tunnel junction which can be adjusted by the bias voltage \( V_b \) weighted by \( C_b \) acts as the threshold value. The function \( F(X) \) for the circuit is given by

\[
F(X) = C^p \sum_{k=1}^{n'} C^p_k V^p_k - C^n \sum_{i=1}^{n} C^n_i V^n_i - T' \tag{4}
\]

\[
T' = \frac{1}{2} \left( C^p + C^n \right) \psi - C_b V_b \tag{5}
\]

In the above expressions, \( C^p = C_b + \sum_{k=1}^{n'} C^p_k \) and \( C^n = C_o + \sum_{i=1}^{n} C^n_i \). The generic threshold gate describe here can be used to implement any logic function. To prevent loading effect as well as to maintain correct voltage levels, SET buffer/inverting are connected at the output of the TLG (11). The circuit of such buffer/inverter is given in Fig. 2.

\[\text{Fig. 1. TLG Gate (a) symbol and (b) structure}\]
SINGLE ELECTRON ENCODED LOGIC GATES AND SYSTEM

The threshold equations for two input AND, OR, NAND and NOR gates can be written as

\[ Y = \text{AND}(a,b) = \text{sgn}\{a+b-2\} \] (6)

\[ Y = \text{OR}(a,b) = \text{sgn}\{a+b-1\} \] (7)

\[ Y = \text{NAND}(a,b) = \text{sgn}\{-a-b+2\} \] (8)

\[ Y = \text{NOR}(a,b) = \text{sgn}\{-a-b+1\} \] (9)

To maximize robustness for variations in parameter values, the threshold value \( T = i \) (i being an integer) can be replaced by the average of the interval (i.e. \( \psi = i-1/2 \) [9] and equations 6 to 9 can be written as

\[ Y = \text{AND}(a,b) = \text{sgn}\{a+b-1.5\} \] (10)

\[ Y = \text{OR}(a,b,c) = \text{sgn}\{a+b+c-0.5\} \] (11)

\[ Y = \text{NAND}(a,b) = \text{sgn}\{-a-b+1.5\} \] (12)

\[ Y = \text{NOR}(a,b) = \text{sgn}\{-a-b+0.5\} \] (13)

The threshold gate implementations of these gates have the same basic circuit topology consisting of a tunnel junction with capacitance \( C_j \), an output capacitor \( C_o \) and a bias capacitor \( C_b \). Additionally AND/OR gates contain two input capacitors \( C_1^p \) and \( C_2^p \) for positively weighted inputs, while the NAND/NOR gates contain two capacitors \( C_1^n \) and \( C_2^n \) for the negatively weighted inputs. The structures of these gates are shown in fig. 3.

To determine the parameter values we assume the following voltage levels: Logic 0=0 V, Logic 1= 0.1e/C=16 mV, \( V_b = 0.1e/C=16 \) mV, \( R_j=100K\Omega \) and \( C_j=0.1C \), where C=1aF is used as a unit of capacitance. Let us first determine the parameter values for AND gate. Since the inputs (A & B) are positive and have equal weights, we choose \( C_1^p = C_2^p = 0.5C \). Given the choice of logic level 1, we want the change in output voltage due to transport of an electron to be equal to 0.1e/C. The change in output voltage due to transport of an electron in direction (y to x) in the generic SET-based TLG is given by [12]
\[ dV_0 = eC_e^p / C_r \]  

(14)

where

\[ C_r = C_e^p C_e^n + C_e^p C_j + C_e^n C_j \]  

(15)

We assume \( C_j \ll C_e^p \) and \( C_j \ll C_e^n \) to ensure that a large percentage of the input voltages are applied over the tunnel junction due to capacitive division and (15) reduces to

\[ C_r = C_e^p C_e^n \]  

(16)

\[ dV_0 = eC_e^p / C_r = e/C_e^p = 0.1e/C \quad \Rightarrow C_e^n = C_0 = 10C \]

If we now apply logic 1 (i.e \( 0.1e/C \)) to all the inputs of the gate, from (4 & 5) we get

\[ F(X)' = C_e^n (C_e^p V_1^p + C_e^n V_2^p) - T' \]

\[ = 10[C(0.5C \times 0.1e/C + 0.5C \times 0.1e/C) - T'] \]

\[ = 0.5eC + 0.5eC - T' = \alpha + \alpha - T' \]

Applying logic 1 to any of the inputs of TLG translate into a contribution of \( \alpha=0.5eC \). Therefore \( \alpha \) act as a scaling factor and \( T \) should also be scaled by \( \alpha \) i.e \( T' = \alpha T = 0.5x1.5eC = 0.75eC \). Substituting this value in (5), we get

\[ 0.75eC = e(C_e^n + C_e^p) / 2 + C_e^n C_0 V_b \]  

(17)

From (17), the value of \( C_b \) is obtained as 9.5C. Using the same procedure, we can determine parameter values for other gates.

As pointed out in ref. 9, a SET buffer/inverter should follow the threshold logic structure to provide enough driving ability and stability. Since the buffer/inverter inverts the output of the original threshold logic, we need to reverse the positively and negatively weighted inputs in the logic function accordingly. The function performed by the buffered gate is the inverse of that performed by the gate itself. For example a buffered AND gate implements the NAND function. The structures for buffered gates are shown in figure 4.

![Figure 4: Buffered Gates](image-url)
The threshold equations for the buffered gates can be written as

\[ Y = \text{Buffered AND}(a, b) = \text{sgn}\{ -a - b + 1.5 \} \] (18)

\[ Y = \text{Buffered OR}(a, b) = \text{sgn}\{ -a - b + 0.5 \} \] (19)

\[ Y = \text{Buffered NAND}(a, b) = \text{sgn}\{ a + b - 1.5 \} \] (20)

\[ Y = \text{Buffered NOR}(a, b, c) = \text{sgn}\{ a + b - 0.5 \} \] (21)

For the 2-input buffered AND gate, \( C^n = C'_1 + C''_2 + C + C_o = 10C \). Assuming \( C'_1 = C''_2 = 0.5C \) we obtained \( C_o = 5C \). From equation (4), the function \( F(X) \) for the buffered gate can be written as

\[ F(X) = -C_b C^n_1 V^n_1 - C_b C''_2 V^n_2 - T' = -0.05eC_b - 0.05eC_b - T' = -\alpha - \alpha - T' \]

Applying logic 1 to any of the inputs of TLG translate into a contribution of \( \alpha = 0.05eC_b \). Therefore \( \alpha \) act as a scaling factor and \( T \) should also be scaled by \( \alpha \) i.e \( T' = -\alpha T = -0.05 \times 1.5eC_b = -0.075eC_b \). When combining a logic gate with buffer/inverter, the buffer adds an additional capacitive load to the logic gate’s output node [9]. The buffer’s supply voltage and output voltage change the logic gate’s biasing due to a feedback effect. This effect is accounted for by considering an additional negatively weighted input \( V^n_{\text{buf}} \) capacitively coupled to the threshold gate with an input capacitance \( C^n_{\text{buf}} \) and the threshold value of each threshold gates must be adjusted by \( -V^n_{\text{buf}} C^n_{\text{buf}} C^n_{\Sigma} \). Therefore, the new threshold is \( T' = -0.075eC_b - 0.046eC_b = -0.121eC_b \). Substituting this value in (5), the value of \( C_b \) is obtained as 13.19C.

The parameter values for the other buffered gates are calculated using the same procedure and the parameters given in Table 1 are obtained.

### Table 1: Parameter values for Buffered Single Electron Encoded Logic Gates

<table>
<thead>
<tr>
<th>GATE</th>
<th>( C_b )</th>
<th>( C_o )</th>
<th>( C_p )</th>
<th>( C_i )</th>
<th>( C_{g1} = C_{g2} )</th>
<th>( C_I = C_4 )</th>
<th>( C_2 = C_3 )</th>
<th>( C_b I = C_{b2} )</th>
<th>( C_l )</th>
</tr>
</thead>
<tbody>
<tr>
<td>2-input AND</td>
<td>13.2</td>
<td>8</td>
<td>-</td>
<td>0.5</td>
<td>0.5</td>
<td>0.5</td>
<td>0.5</td>
<td>0.1</td>
<td>4.25</td>
</tr>
<tr>
<td>2-input OR</td>
<td>10.6</td>
<td>9</td>
<td>0.5</td>
<td>-</td>
<td>0.5</td>
<td>0.5</td>
<td>0.5</td>
<td>0.1</td>
<td>4.25</td>
</tr>
<tr>
<td>2-input NAND</td>
<td>11.7</td>
<td>9</td>
<td>0.5</td>
<td>-</td>
<td>0.5</td>
<td>0.5</td>
<td>0.5</td>
<td>0.1</td>
<td>4.25</td>
</tr>
<tr>
<td>3-input OR</td>
<td>11.8</td>
<td>7.8</td>
<td>0.4</td>
<td>0.5</td>
<td>0.5</td>
<td>0.5</td>
<td>0.5</td>
<td>0.1</td>
<td>4.25</td>
</tr>
</tbody>
</table>

To confirm the feasibility of using the above gates in a system, the gates were used to implement the Boolean function \( Y = AB + C + D \).

**RESULTS AND DISCUSSION**

The performance of the buffered gates, required for implementation of the Boolean function \( Y = AB + C + D \) are simulated using Monte Carlo simulation software SIMON2. The simulated circuits and their input-output waveforms are shown in figures 5 to 7. The results obtained from the simulation are found to be satisfactory.
The digital system given by the Boolean function \( Y = AB + C + D \) is implemented using the gates designed above. The complete circuit implemented using SIMON2 is given in Fig. 8 and the waveforms are given in Fig. 9.
The results obtained from the simulation are found to be satisfactory. The stability of the circuit is studied by constructing its free energy history diagrams and its stability plots. Fig. 10 shows the free energy history, when electron is transported from the output node N2 to Vss through J1 and J2, leaving a positive charge in N2 and changing the value of the output from 0 to 1. Initially there is no charge in N2 and the free energy is zero. During the second time step, an electron is transported from island N2 to island N1 through J2 and the free energy increases. During the third time step, the electron is transported from island N1 to Vs through J1 and there is significant decrease in free energy. At this point the output N2 is positively charged and we have a transition from 0 to 1. Both logic 0 and logic 1 states correspond to energy minima. This is a strong indication of gate stability.

Fig. 10. Free energy history

![Free energy history diagram](image)

To confirm the stable operation of the single-electron circuit, its stability plots have been constructed using SIMON2. Fig. 11 shows two dimensional sections of the stability plot. With A and B equal to 0, the four possible combinations of the values of the other two inputs (C & D) are represented by points 1, 2, 3 and 4. The points 5, 6, 7 and 8 represents the four possible combinations of C and D with A=0 and B=16mV. All the 16 possible combinations of the inputs are represented by the points 1 to 16 in Figs 9(a) to 9(d). It is clear that all points 1–16 are located into stable regions, i.e. in white, which are stable enough to allow the desired operation of the circuit shown in Fig. 8.

Fig. 11. Stability plots of the single electron circuit, C versus D; (a) A=0V & B=0V, (b) A=0V, B=16mV, (c) A=16mV, B=0V and (d) A=16mV, B=16mV

![Stability plots diagram](image)
CONCLUSION
The design and simulation of a single-electron encoded logic gates and system are presented. The performance of the gates and system are verified using SIMON2. The free energy history diagrams and stability plots show that the system presented in this paper is stable thereby establishing the feasibility of using single electron encoded logic gates in future low power ultra-dense VLSI circuits.

ACKNOWLEDGEMENT
The author thankfully acknowledges the financial supports obtained from MIT under AICTE-NEQIP grant.

REFERENCES
13. C. Lageweg and S.