Germanium-Silicon Based Hetero Junction Cylindrical Gate All Around Field Effect Transistor for Improved Performance

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ABSTRACT
Performance analysis of a hetero junction cylindrical gate all around field effect transistor (HJ-CGAA FET) is reported in this paper where source-drain material is germanium (Ge) and silicon (Si) is used as channel material. We also replaced the traditional silicon-di-oxide(SiO$_2$) layer with silicon nitride (Si$_3$N$_4$). The simulation results indicate that this hetero junction structure is able to provide an improved performance over a conventional cylindrical gate all around FET. An optimized DIBL of 75.5167 mV/V and SS of 68.2 mV/dec is achieved for 10nm technology node from TCAD simulation. Other performance parameters are also calculated which anticipates that this FET can be scaled down up to 5nm while maintaining a better On-Off current ratio.

Keywords  
hetero junction cylindrical gate all around FET, scaling, drain induced barrier lowering, subthreshold swing, silicon nitride

INTRODUCTION
In order to integrate more numbers of transistor in a single chip, field effect transistors (FET) are required to downscale invasively. However, downscaling the conventional planner FET has become a major challenge to device engineers as shorter channel FETs has some serious issues like short channel effects (SCEs), degraded subthreshold swing (SS), higher Off current (I$_{off}$) [1-3]. Among these SCEs drain induced barrier lowering (DIBL) affects the I$_{off}$ and SS by a large amount which needs to be optimized as much as possible. Many techniques to solve these problems of shorter channel FETs has been introduced over the decades like changing the FET structure, introducing new channel-source-drain materials, High-K dielectrics as oxide layer etc. [4]. However, gate all around FET provides the highest electrostatic control over the flow of the current and manages to scale down the FET further compared to double-gate, tri-gate, quadruple-gate, omega-gate, p-gate FETs [13,14]. In addition, indium arsenide (InAs), germanium (Ge), gallium nitride (GaN), gallium arsenide (GaAs) and graphene can be the alternative materials to silicon (Si) for manufacturing the field effect transistors [5-8]. This work focuses on hetero junction cylindrical gate all around (HJ-CGAA)FET having Silicon and Germanium as channel and source-drain (S-D) materials respectively. Silicon Nitride (Si$_3$N$_4$) is used as the oxide material in this HJ-CGAA FET which ensures large coupling capacitance, high chemical stability over silicon-di-oxide (SiO$_2$) and high melting point [9]. Thus, a strong electric field is produced and uniformly distributed over the channel which confirms excellent gate control over the flow of current. Pure Ge delivers more than 2x mobility for electrons compared to Si [12] which is why Ge is preferred as S-D over Si. Silicon has intrinsic carrier concentration (ICC) of 1.45x10$^{10}$ cm$^{-3}$ [10] which is much lower than the ICC of Ge 2.4x10$^{13}$ cm$^{-3}$ [10]. Because of this lower intrinsic carrier concentration Si provides lower off state current. If we combine all of these advantages together we may expect, lower I$_{off}$, higher On-Off current ratio, better
SS and an optimized DIBL effect after this modification. Our simulation results also reveal that an improved performance up to 5nm technology node can be achieved with HJ-CGAA FET.

DEVICE STRUCTURE AND SIMULATION

3D HJ-CGAA FET is demonstrated in fig.1 where 1(a) shows the 3D full view and 1(b) shows the quarter view of the device.

Fig1: (a) 3D full view of the HJ-CGAA-FET (b) quarter view of the device

The device has Ge source and drain of uniform doping of 1x10^{20} cm^{-3} and Si channel has a doping concentration of 1x10^{19} cm^{-3}. A metal gate of work function 5eV is used to encircle the silicon nanowire channel along with a 1nm thickness of Si_{3}N_{4} oxide layer. The device has a channel thickness of 5nm along diameter. The simulations were conducted using ATLAS tool of Silvaco TCAD software by taking an ultra-thin 2D slice from the 3D structure shown in fig. 2.

Fig2: 2D slice along diameter
First Schrodinger equation was solved to determine the eigenfunction and eigenvalues at each slice and then non-equilibrium Greens function (NEGF) was solved using mode-space approach to determine the quantum transport of the device. Three different node sizes of 10nm, 7nm and 5nm was studied to analyze the performance of the FET.

SIMULATION RESULTS AND DISCUSSION

Transfer characteristics and other performance parameters generated from ATLAS Silvaco TCAD simulation are demonstrated and discussed in this section. Transfer characteristics of 10nm HJ-CGAA FET for two different drain voltage ($V_D$) is shown in Fig.3 which clearly reveals that not only off-state current is extremely low but the device also has a higher on state current. The linear region slope is sharp enough that determines an excellent On-Off current ratio and SS as well. The curve also explains that the $I_{off}$ of 10nm HJ-CGAA is less sensitive to $V_D$. Good electrostatic control over the channel, lower ICC of Si during no bias condition and novel electron transport capability of Ge S-D are the key reasons behind this enhanced transfer characteristics.

Fig 3: Transfer characteristics of 10nm JL-DCGAA-FET

Fig.4 and Fig.5 demonstrates the transfer characteristics of the HJ-CGAA FET of node size 7nm and 5nm respectively. In case of 5nm and 7nm node the On-Off current ratios are in acceptable range. The high-k dielectric $\text{Si}_3\text{N}_4$ creates a large coupling capacitance which results a well distributed strong electric field over the channel. Thus, number of transport carriers change dramatically when gate bias is applied which is why a sharp linear region slope is achieved. Though 7nm and 5nm node size shows off state current that is not immune to increase in $V_D$, but it still allows the FET to scale below 10nm.

Fig 4: Transfer characteristics of 10nm JL-DCGAA-FET
Table 1 shows the performance parameters of the 10nm node where we can see that a SS of 68.2 mV/dec can be accomplished by 10nm HJ-CGAA FET which is better than 10nm GAA performed by P Zheng et. al [11]. The DIBL problem is greatly optimized in this structure. Only a DIBL of 75.5167 mv/V is obtained from a 10nm HJ-CGAA FET. To verify the claim of this optimized DIBL, the band diagrams of 10nm HJ-CGAA FET for zero gate biasing condition across source-channel-drain region is shown in fig.6 and fig.7. These two figures demonstrate the conduction band energy for two different drain voltages 0.05V and 0.8V respectively. It is clear from fig.6 and fig.7 that the barrier height at source end decreases negligibly for increasing the drain voltage which is why HJ-CGAA FET manages to suppress the DIBL by a large amount.
An impressive SS, on current, off current and on-off current ratio is reported in table 2&3 for 7 and 5nm node size respectively. Only 0.7V is required as gate bias to attain an $I_{on}$ of 2.96uA from a 5nm technology node that elicits HJ-CGAA FET can be a solution to minimize the static power for shorter channel FET as the supply voltage is extremely in low range. The on-off current ratio for 7nm HJ-CGAA FET is greater than $10^8$ that explains the reason of getting an improved SS of 85.1mV/dec. The device manages a higher on-off current ratio ($>10^4$) for even 5nm node size which proves the scalability and possibility of the device for shorter channel length.

Table 1. Performance parameters for 10, 7 and 5nm JL-CGAA FET for $V_D=0.05V$

<table>
<thead>
<tr>
<th>Parameters</th>
<th>10nm</th>
<th>7nm</th>
<th>5nm</th>
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<tr>
<td>$I_{on}$ (A)</td>
<td>1.68E-06</td>
<td>2.76E-06</td>
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<td>$I_{off}$ (A)</td>
<td>1.69E-18</td>
<td>9.24E-15</td>
<td>1.87E-11</td>
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<td>$I_{on}/I_{off}$</td>
<td>9.94E+11</td>
<td>2.99E+08</td>
<td>5.67E+04</td>
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<td>SS (mV/dec)</td>
<td>68.2</td>
<td>85.1</td>
<td>113.8</td>
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<td>DIBL (mV/V)</td>
<td>75.5167</td>
<td>104.367</td>
<td>283.997</td>
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</table>

Table 2: Performance parameters for 10, 7 and 5nm JL-CGAA FET for $V_D=0.8V$

<table>
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<tr>
<td>$I_{on}$ (A)</td>
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<td>$I_{off}$ (A)</td>
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<td>3.31E-10</td>
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<tr>
<td>$I_{on}/I_{off}$</td>
<td>3.51E+11</td>
<td>1.41E+07</td>
<td>8.94E+03</td>
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<td>SS (mV/dec)</td>
<td>70.4</td>
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CONCLUSION
A Ge-Si based hetero junction cylindrical gate all around FET having Si₃N₄ as oxide is studied in this work. To investigate the performance of this FET, ATLAS Silvaco TCAD simulation was conducted for three different node sizes 10, 7 and 5nm. The device shows an improved performance in terms of On-off current ratio, SS and DIBL over conventional cylindrical gate all around FET. The deterioration of its performance parameters with the decrease of the node size is in an acceptable limit which makes this FET superior compared to single, multi-gate and gate all around homojunction devices.

REFERENCES